(c) a lateral growth on said gate dielectric at the corners of said gate, but not under central regions of said gate increasing the thickness of said gate dielectric at the interface of said bottom surface and said sidewalls;

(d) a unitary electrically conductive metallic material entirely covering said sidewalls and top surface of said gate; and

(e) source and drain regions in said semiconductor region defining a channel under said patterned gate.

Amend claim 9 as follows:

9. (Four Times Amended) A transistor gate structure, comprising:

(a) a gate dielectric over a semiconductor region;

(b) a patterned gate over said gate dielectric having sidewalls, a top surface and a bottom surface disposed on said gate dielectric;

(c) a lateral growth on said gate dielectric at the corners of said gate, but not under central regions of said gate increasing the thickness of said gate dielectric at the interface of said bottom surface and said sidewalls; and

(d) a unitary electrically conductive metallic material entirely covering said sidewalls and top surface of said gate.

Amend claim 10 as follows:

10. (Amended) A transistor structure which comprises:

a region of semiconductor material having a gate dielectric thereover;

a polysilicon gate disposed over said gate dielectric having a top and sidewalls;

a silicide layer disposed on said top and sidewalls of said polysilicon gate; and

source/drain regions in said region of semiconductor material spaced apart from each other and each disposed adjacent to and aligned with [a] said silicide layer disposed on said sidewalls [polysilicon gate sidewall; and

a silicide layer disposed on said top and sidewalls of said polysilicon gate].

Cancel claims 11, 13, 15, 17, 19, 21, 23 and 25 without prejudice.

REMARKS

Claims 8 to 10 have been amended and claims 11, 13, 15, 17, 19, 21, 23 and 25 have been cancelled. Claims 8 to 10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 remain active in this application.

Claims 8, 9, 11, 13, 15, 17, 19, 21, 13 and 25 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, the examiner referring specifically to the recitation "entirely covering said gate". The rejection is respectfully traversed.

The specification clearly states at page 4, lines 19 to 21 that "[t]he sidewalls of the gate are then exposed and a metal for siliciding is deposited overall, after which source/drain implants are performed." At page 8, lines 4 to 6, it is clearly stated that "[t]his is followed by conformal